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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/756,853 | 01/14/2004 | Norman Rubin | 00100.03.0023 | 3409 |

29153 7590 04/05/2006

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| EXAMINER | |
|---|---|
| LAI, VINCENT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2181 | |

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/756,853 | RUBIN ET AL. | |
| | Examiner | Art Unit | |
| | Vincent Lai | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *1/14/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
AU2181 4/1/2006

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on May 21, 2004 was considered by the examiner.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method and Apparatus for Nested Control Flow Utilizing Extra Bits as Context Information and a Counter Indicating Nesting Depth."

### *Claim Objections*

3. Claim 19 is objected to because of the following informalities:

In claim 19, there is an extraneous period in the last sentence of the claim. It is suggested to be removed.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

*4.* Claims 1, 6, 11, 13, 16, and 19-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. There are no tangible end results from implementing the claims in question because the end result is a determination, which lacks a tangible "real world" result. Although some claims do have intermediate steps that produce an intermediate tangible result, the end result is merely a determination. It is recognized that some of the claims will not always end with a determination, but since there is no way to ensure that a determination is not the final step in those claims, the claims are still directed to non-statutory subject matter.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 6, 8-9, 11-14, 16-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Witt (U.S. Patent # 6,061,786), herein referred to as Witt.

As per claim 1, Witt discloses a method for nested control flow (See column 2, lines 7-9: A control flow change is called a control transfer), the method comprising:

setting a context bit (Control transfer bit: see column 6, lines 27-30) to at least one of: a first state and a second state (See column 6, lines 29-31: The two states are

branch or not branch) receiving a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

determining whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares); and if the context bit is read, executing the instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other).

As per claim 2, Witt discloses further comprising: upon the executing of the first instruction, maintaining a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per claim 6, Witt discloses further comprising:

receiving a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

determining whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

if the context bit is read, executing the instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other);

and upon executing the second instruction, maintaining the counter (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per claim 8, Witt discloses an apparatus for nested control flow (See column 2, lines 7-9: A control flow change is called a control transfer), the apparatus comprising:

a processor (Processor 10, see figure 1) having a context bit (Control transfer bit: see column 6, lines 27-30);

a first memory device storing a plurality of instructions (See figure 1, and column 5, lines 30-42: An instruction cache is present), wherein each of the plurality of instructions includes a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information), the processor operative to execute the plurality of instructions (All processors can execute instructions); and

a second memory device operably coupled to the processor, the memory device receiving an incrementing counter instruction upon the execution of one of the plurality of instructions (See column 15, lines 59-65: A counter is used with increments when a branch is taken).

As per claim 9, Witt discloses further comprising: a context bit memory device capable of storing the context bit (See figure 5: The context bits are saved in a register).

As per claim 11, Witt discloses wherein the processor receives a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information) from the memory and the processor determines whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares).

As per claim 12, Witt discloses wherein the processor executes the first instruction when the context bit is read (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other) and is in a first state and the processor maintaining a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state, in response to the incrementing counter instruction (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per claim 13, Witt discloses wherein the process receives a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information) from the memory and the processor determines whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares) and if the context bit is read, executing the second instruction when the context bit is in a first state and incrementing the counter bit in response to the incrementing counter instruction (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other).

As per claim 14, Witt discloses a graphics processing device comprising:

a plurality of arithmetic logic units (See column 11, lines 22-25: The functional units are responsible for execution of instructions and thus will inherently have at least one ALU), each of the plurality of arithmetic logic units having a context bit memory device capable of storing a context bit (Control transfer bit: see column 6, lines 27-30);

a first memory device storing a plurality of instructions (See figure 1, and column 5, lines 30-42: An instruction cache is present), wherein each of the plurality of instructions includes a plurality of extra bits See column 6, lines 14-15: There are two bits of predecode information), the arithmetic logic units operative to execute the plurality of instructions (All ALUs execute instructions); and

a second memory device operably coupled to the processor, the second memory device receiving an incrementing counter instruction upon the execution of one of the plurality of instructions (See column 15, lines 59-65: A counter is used with increments when a branch is taken).

As per claim 16, Witt discloses wherein each of the plurality of arithmetic logic units receive at least one of the plurality of instructions and the arithmetic logic units determine whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares).

As per claim 17, Witt discloses wherein the plurality of arithmetic logic units execute the instructions when the context bit is read (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other) and is in a first state and maintaining a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state, in response to the incrementing counter instruction (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per claim 19, Witt discloses a method for nested control flow, the method comprising:

setting a context bit (Control transfer bit: see column 6, lines 27-30) to at least one of: a first state and a second state (See column 6, lines 29-31: The two states are branch or not branch) receiving a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

determining whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

if the context bit is read, executing the instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other); and

upon the executing of the first instruction (See column 15, lines 59-62: The bimodal counter), wherein the counter value indicates a nesting depth of context bits

that are set to a second state (See column 15, lines 62-65: The counter is incremented when a branch is taken) in a general purpose register.

As per claim 20, Witt discloses further comprising:

receiving a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

determining whether to read the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

if the context bit is read, executing the instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other);

and upon executing the second instruction, incrementing the counter (See column 15, lines 62-65: The counter is incremented when a branch is taken).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-4, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (U.S. Patent # 6,061,786), herein referred to as Witt.

As per claims 3-4, 10 and 15, Witt teaches the use of a counter (See column 15, lines 59-62).

Witt does not teach storing a counter or the means to store a counter.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store a counter in a non-dedicated memory device, wherein the non-dedicated memory device is a general purpose register. Storing a counter in a register is one of the simplest methods used and has been readily done in the field.

7. Claims 5, 7, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (U.S. Patent # 6,061,786), herein referred to as Witt in view of Poland et al (U.S. Patent # 5,673,407), herein referred to as Poland et al.

As per claim 5, Witt teaches the use of a context bit (Control transfer bit: see column 6, lines 27-30).

Witt does not teach resetting the counter value.

Poland et al teaches prior to setting the context bit, resetting the counter value (See column 14, lines 36-39: Values are reloaded after being zeroed at the end of an operation thus meaning a new context is necessary).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reset the counter value since an incorrect counter would be of no use to determining a count and would be counterproductive.

As per claim 7, 18, and 21, Witt teaches the use of a counter (See column 15, lines 59-62),

Witt does not teach terminating a computation processing using the counter

Poland et al teaches terminating a computation processing using the counter (See column 14, lines 33-44: The counter is used as a timer as well and such a termination can be done with a time-out timer/counter).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to allow termination of processes using a counter because unchecked processes can tie up valuable resources/computation time, which would thus take away from any benefits the invention is meant to make.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to show further art related to method and apparatus for nested control flow utilizing extra bits as context information and a counter indicating nesting depth:

U.S. Patent # 5,692,168 to McMahan shows a prefetch buffer using flow control bit to identify changes of flow within the code stream.

U.S. Patent # 6,321,302 B1 to Strongin et al shows a stream read buffer for efficient interface with block oriented devices.

U.S. Patent # 6,717,576 B1 to Duluk, Jr. et al shows deferred shading graphics pipeline processing having advanced features.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
March 31, 2006

Supervisory

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4/1/2006